REMARKS

The Examiner has objected to the drawings. Applicant files herewith corrected formal drawings. The text descriptions on sheets 1, 2, 4, 5 and 6, and also on sheets 7, 8, 9 and 11 has been deleted, as proposed by the Examiner. The reference sign "C3" has been changed to "C2" in Figure 8(a) and the reference sign "T2" has been added to Figure 9(a).

Applicant respectfully submits that the changes that have been made overcome the objections to the drawings.

In regard to the objection made in paragraph 2 of the Office Action, Applicant has provided an abstract of the disclosure.

In paragraph 3 of the Office Action, the Examiner has objected that the specification fails to provide proper antecedent basis for the claimed subject matter. The "inverted gate means" recited in claims 19 and 23 is described with reference to the Figure 10 embodiment. Applicant respectfully requests amendment of the specification at page 11, line 8, to make clear that:

> Figure 10 shows a further embodiment of the invention in which inverted gate means in the form of a NOT gate U4 is used as a fast switching comparator.

Applicant respectfully submits that the amended specification clearly identifies the element shown in the drawings that corresponds to the recited claim language.

The Examiner has also objected that the specification does not provide proper antecedent basis for the feature of "means providing a low impedance path between the input and the output of the negative feedback path" as recited in claim 25. Applicant respectfully submits that structure corresponding to this claimed feature is plainly described at page 5, lines 17 to 19, of the specification and at page 14, lines 12 to 15; namely, the optional speedup diodes, D5 to D8.

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Applicant respectfully submits that the amended specification clearly identifies the structure shown in the drawings that corresponds to the recited claim language.

In paragraph 4 of the Office Action, the Examiner has objected to certain alleged informalities in the disclosure. With a view to overcoming these objections, Applicant requests that the expression "8 and 9" at page 3, line 16, be changed to --8a and 9a-- and requests correction of Figure 9(a) on sheet 11/12 of the drawings to show "transistor T2."

However, Applicant does not, with respect, agree that "(R1,C4)," on page 4, at line 14, be changed to --(R2,C4)--. As described at page 4, lines 13 to 16, the anti-jitter circuit has a low pass filter which is connected to the integrator storage capacitor C3. This low pass filter is defined by resistor R1 and capacitor C4, as correctly described at page 4, line 14. The resistor R2 connected to the collector of transistor T1 is not part of the low pass filter. In fact, as described at page 5, lines 8 and 9 the circuit time constant depends on R1 and C4; the time constant does not depend on R2 which is not part of the low pass filter.

In paragraph 6 of the Office Action the Examiner has objected to certain alleged informalities in claims 12, 27 and 30.

In regard to claim 12, Applicant requests that the expression "mean d.c. level" be changed to --mean dc voltage level--, as proposed by the Examiner. However, Applicant does not, with respect, agree with the Examiner that the expression "a discharge part" be changed to "the voltage level" in claim 12, at line 2. Although the "means for comparing," recited in claim 1, produces output pulses whenever both the charge (i.e., rising) and discharge (i.e., falling) parts of the time-varying voltage waveform cross the mean d.c. voltage level, the monostable circuit defined in claim 12 is only triggered whenever the discharge part of the time-varying voltage waveform crosses the mean d.c. voltage level,

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because the discharge part of the waveform has much reduced time jitter. This is disclosed at page 5, lines 1 to 4 of the specification.

In regard to the objection made in relation to claim 27, Applicant has deleted "the or each" in line 1, and has amended the claim to be dependent on claim 1 only.

Applicant has also corrected the spelling of "combination" in claim 30.

In paragraph 7 of the Office Action, claims 1 to 27 and 29 to 30 stand rejected under 35 U.S.C. § 112, second paragraph, as being allegedly indefinite "for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention."

Applicant respectfully requests that claim 1 be amended to include the expression --for storing charge-- after "integrator charge storage means" to complete the means plus function statement as required by 35 U.S.C. § 112, sixth paragraph.

Applicant also requests that the feature of "a low pass filter coupled to said integrator charge storage means for deriving a mean d.c. voltage level of said time varying voltage waveform" be included in independent claim 1. Applicant respectfully submits that this amendment overcomes the rejection of claim 1 under 35 U.S.C. § 112, second paragraph.

The Examiner suggests that the low pass filter of Figure 6 is defined by resistor R2 and capacitor C4. In fact, as already explained in connection with the Examiner's proposed amendment to page 4 at line 14, the low pass filter is defined by resistor R1 and capacitor C4.

The Examiner alleges that the recitation "means defining a negative feedback path ... integrator charge storage" in claim 2 is misdescriptive. Applicant does not with respect agree. As described at page 4, lines 13 to 16, the low pass filter defined by resistor R1 and capacitor C4 and connected to the integrator storage capacitor C3 "controls the discharge

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current in a negative feedback configuration" (emphasis added). This is also described in the passage bridging pages 13 and 14.

The Examiner alleges that the recitation of "frequency doubling means" is "misdescriptive" and that the claim is allegedly indefinite. Applicant requests that claim 13 be amended to recite that the "first and second charging means" are "effective as a frequency doubling means." Applicant respectfully submits that this amendment overcomes the Examiner's rejection of claim 13.

The Examiner has rejected claims 19, 20, 23 and 24 as being allegedly unclear. Applicant does not, with respect, agree. As already explained, in response to the objection made in paragraph 3 of the Office Action, the "inverted gate means" recited in claims 19 to 24 is described with reference to the Figure 10 embodiment as NOT gate U4 which has an input coupled to integrator charge storage means (capacitor C3) and an output, as required by the rejected claims.

The Examiner has rejected claim 25 as being allegedly unclear. As already explained in response to the objection made in paragraph 3 of the Office action, structure corresponding to "means providing a low impedance path ..." recited in this claim is disclosed at page 5, lines 17 to 19, of the specification and at page 14, lines 12 to 15; namely, the optional speedup diodes D5 to D8.

Applicant notes from paragraph 8 of the Office Action that claim 1 and the dependent claims are allowable in relation to the prior art.

In view of the foregoing amendments and remarks Applicant submits, with respect, that the amended claims overcome all the objections made by the Examiner. The application is considered in good and proper form for allowance and the Examiner is

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respectfully requested to pass the application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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